3. (Amended) A method of manufacturing a semiconductor device comprising at least two p-channel thin film transistors,

each of the two p-channel thin film transistors fabricated through the method comprising:

forming a semiconductor island over a substrate;

forming a gate electrode adjacent to the semiconductor island with a gate insulating film therebetween;

forming a source region, a drain region and a channel region formed between the source and drain regions,

wherein the two p-channel thin film transistors are connected in series,

wherein an off current from each of the p-channel thin film transistors is less than 10^{-12} A where a voltage of the drain region is 1V.

4. (Amended) A method according to claim 3, further comprising:

forming an interlayer insulating film including boro-phosphosilicate glass over the two p-channel thin film transistors.

5. (Amended) A method according to claim 3, wherein the semiconductor island is a crystalline semiconductor island.

6. (Amended) A method according to claim 3, wherein each of the source and drain regions comprises boron.

8. (Amended) A method according to claim 9 further comprising:

forming a blocking film between the substrate and the semiconductor island,

wherein the substrate is a glass substrate;

wherein the blocking film includes,

a silicon nitride film with a thickness in a range of 5-200 nm formed on the glass substrate, and

a silicon oxide film with a thickness in a range of 20-1000 nm formed on the silicon nitride film.

9. (Amended) A method of manufacturing a display device, said display device comprising:

a pixel portion and a driving circuit portion;

at least two p-channel thin film transistors being formed in the pixel portion;

each of the two p-channel thin film transistors fabricated through the method comprising:

forming a semiconductor island over a substrate;

forming a gate electrode adjacent to the semiconductor island with a gate insulating film therebetween;

forming a source region, a drain region and a channel region formed between the source and drain regions,

wherein the two p-channel thin film transistors are connected in series,

wherein an off current from each of the p-channel thin film transistors is less than 10^{-12} A where a voltage of the drain region is 1V.

10. (Amended) A method according to claim 9, further comprising:

forming an interlayer insulating film including boro-phosphosilicate glass over the two p-channel thin film transistors.

11. (Amended) A method according to claim 9, wherein the semiconductor island is a crystalline semiconductor island.

12. (Amended) A device according to claim 9, wherein each of the source and drain regions comprises boron.

14. (Amended) A method according to claim 15 further comprising:

forming a blocking film between the substrate and the semiconductor island,

wherein the substrate is a glass substrate,

wherein the blocking film includes,

a silicon nitride film with a thickness in a range of 5-200 nm formed on the glass substrate, and

a silicon oxide film with a thickness in a range of 20-1000 nm formed on the silicon nitride film.

15. (Amended) A method of manufacturing a semiconductor device, said semiconductor device comprising:

at least a first p-channel thin film transistor and a second p-channel thin film transistor;

a transmission gate including a CMOS circuit, said CMOS circuit including at least an n-channel thin film transistor and a third p-channel thin film transistor;

each of the first, second and third p-channel thin film transistors fabricated through the method comprising:

forming a semiconductor island over a substrate;

forming a gate electrode adjacent to the semiconductor island with a gate insulating film therebetween;

forming a source region, a drain region and a channel region formed between the source and drain regions,

wherein the first and second p-channel thin film transistors are connected in series,

wherein an off current from each of the first, second and third p-channel thin film transistors is less than 10^{-12} A where a voltage of the drain region is 1V.

16. (Amended) A method according to claim 15 further comprising:

forming an interlayer insulating film including boro-phosphosilicate glass over the first, second and third p-channel thin film transistors and the n-channel thin film transistor.

17. (Amended) A method according to claim 15, wherein the semiconductor island is a crystalline semiconductor island.

18. (Amended) A method according to claim 15, wherein each of the source and drain regions of each of the first, second and third p-channel thin film transistors comprises boron.

19. (Amended) A method according to claim 15, wherein each of the second source and drain regions of the n-channel thin film transistor comprises phosphorus.

Please add new claims 20-42.

--20. A method of manufacturing a semiconductor device comprising at least two p-channel thin film transistors,

each of the two p-channel thin film transistors fabricated through the method comprising:

forming an amorphous semiconductor film on an insulating surface over a substrate;

crystallizing the amorphous semiconductor film to form a crystalline semiconductor film;

patterning the crystalline semiconductor film to form a crystalline semiconductor island;

forming a gate electrode adjacent to the crystalline semiconductor island with a gate insulating film therebetween;

introducing a p-type impurity to form a source region, a drain region and a channel region formed between the source and drain regions,

wherein the two p-channel thin film transistors are connected in series,

wherein an off current from each of the p-channel thin film transistors is less than 10^{-12} A where a voltage of the drain region is 1V.

21. A method according to claim 20, further comprising:

forming a blocking film between the substrate and the crystalline semiconductor island,

wherein the substrate is a glass substrate;

wherein the blocking film includes,

a silicon nitride film with a thickness in a range of 5-200 nm formed on the glass substrate, and

a silicon oxide film with a thickness in a range of 20-1000 nm formed on the silicon nitride film.

22. A method according to claim 20, further comprising:

forming an interlayer insulating film including boro-phosphosilicate glass over the two p-channel thin film transistors.

23. A method according to claim 20, wherein each of the source and drain regions comprises boron.

24. A method according to claim 20, wherein the amorphous semiconductor film is crystallized by thermally annealing.

25. A method of manufacturing a semiconductor device comprising at least two p-channel thin film transistors,

each of the two p-channel thin film transistors fabricated through the method comprising:

forming an amorphous semiconductor film on an insulating surface over a substrate;

annealing the amorphous semiconductor film with a laser light to crystallize the amorphous semiconductor film;

patterning the crystallized semiconductor film to form a crystalline semiconductor island;

forming a gate electrode adjacent to the crystalline semiconductor island with a gate insulating film therebetween;

introducing a p-type impurity to form a source region, a drain region and a channel region formed between the source and drain regions,

wherein the two p-channel thin film transistors are connected in series,

wherein an off current from each of the p-channel thin film transistors is less than 10^{-12} A where a voltage of the drain region is 1V.

26. A method according to claim 25, further comprising:

forming a blocking film between the substrate and the crystalline semiconductor island,

wherein the substrate is a glass substrate;

wherein the blocking film includes,

a silicon nitride film with a thickness in a range of 5-200 nm formed on the glass substrate, and

a silicon oxide film with a thickness in a range of 20-1000 nm formed on the silicon nitride film.

27. A method according to claim 25, further comprising:

forming an interlayer insulating film including boro-phosphosilicate glass over the two p-channel thin film transistors.

28. A method according to claim 25, wherein each of the source and drain regions comprises boron.

29. A method of manufacturing a semiconductor device comprising a plurality of p-channel thin film transistors,

each of the plurality of the p-channel thin film transistors fabricated through the method comprising:

forming a semiconductor island over a substrate;

forming a gate electrode adjacent to the semiconductor island with a gate insulating film therebetween;

forming a source region, a drain region and a channel region formed between the source and drain regions,

wherein the plurality of p-channel thin film transistors are connected in series,

wherein an off current from each of plurality of the p-channel thin film transistors is less than 10^{-12} A where a voltage of the drain region is 1V.

30. A method according to claim 29, further comprising:

forming a blocking film between the substrate and the semiconductor island,

wherein the substrate is a glass substrate;

wherein the blocking film includes,

a silicon nitride film with a thickness in a range of 5-200 nm formed on the glass substrate, and

a silicon oxide film with a thickness in a range of 20-1000 nm formed on the silicon nitride film.

31. A method according to claim 29, further comprising:

forming an interlayer insulating film including boro-phosphosilicate glass over the two p-channel thin film transistors.

32. A method according to claim 29, wherein the semiconductor island is a crystalline semiconductor island.

33. A method according to claim 29, wherein each of the source and drain regions comprises boron.

34. A method according to claim 29, wherein the semiconductor device includes at least three p-channel thin film transistors connected in series.

35. A method of manufacturing a display device,

said display device comprising:

a pixel portion;

a drive circuit portion;

at least a first p-channel thin film transistor and a second p-channel thin film transistor in the pixel portion;

a transmission gate including a CMOS circuit in the drive circuit portion, said CMOS circuit including at least an n-channel thin film transistor and a third p-channel thin film transistor;

each of the first, second and third p-channel thin film transistors fabricated through the method comprising:

forming a semiconductor island over a substrate;

forming a gate electrode adjacent to the semiconductor island with a gate insulating film therebetween;

forming a source region, a drain region and a channel region formed between the source and drain regions,

wherein the first and second p-channel thin film transistors are connected in series,

wherein an off current from each of the first, second and third p-channel thin film transistors is less than 10^{-12} A where a voltage of the drain region is 1V,

wherein only p-channel thin film transistors connected in series are used as a switching element in the pixel portion.

36. A method according to claim 35 further comprising:

forming an interlayer insulating film including boro-phosphosilicate glass over the first, second and third p-channel thin film transistors and the n-channel thin film transistor.

37. A method according to claim 35, wherein the semiconductor island is a crystalline semiconductor island.

38. A method according to claim 35, wherein each of the source and drain regions of each of the first, second and third p-channel thin film transistors comprises boron.

39. A method according to claim 35, wherein each of the second source and drain regions of the n-channel thin film transistor comprises phosphorus.

40. A method of manufacturing a semiconductor device comprising:

forming a semiconductor film comprising amorphous silicon on an insulating surface;

heating the semiconductor film to crystallize said semiconductor film at least partly;

patterning the crystallized semiconductor film into at least first and second semiconductor islands;

forming a gate insulating film on the first and second semiconductor islands;

forming source and drain regions having a p-type conductivity in the first and second semiconductor islands wherein a channel region is formed between the source and drain regions in the first and second semiconductor islands;

forming at least first and second p-channel thin film transistors wherein said first and second p-channel thin film transistors using said first and second semiconductor islands as active layers thereof;

wherein each of the first and second semiconductor islands has a first portion which includes said channel region and has a crystalline structure and a second portion having an amorphous structure below the first portion.

41. A method according to claim 39 wherein the first and second p-channel thin film transistors are connected to a pixel electrode in series.

42. A method according to claim 39 wherein an off current of each of the first and second p-channel thin film transistors is 10^{-12} A when a voltage of the drain region is 1V.--